(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 270 191**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 87202388.2

(22) Date of filing: 02.12.87

(51) Int. Cl.⁴: H03K 23/00 , H03K 5/15

(30) Priority: 05.12.86 GB 8629108

(43) Date of publication of application:
08.06.88 Bulletin 88/23

(84) Designated Contracting States:
DE FR GB IT NL

(71) Applicant: PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED
Arundel Great Court 8 Arundel Street
London WC2R 3DT(GB)

(84) GB

(71) Applicant: N.V. Philips' Gloeilampenfabrieken
Groenewoudseweg 1
NL-5621 BA Eindhoven(NL)

(84) DE FR IT NL

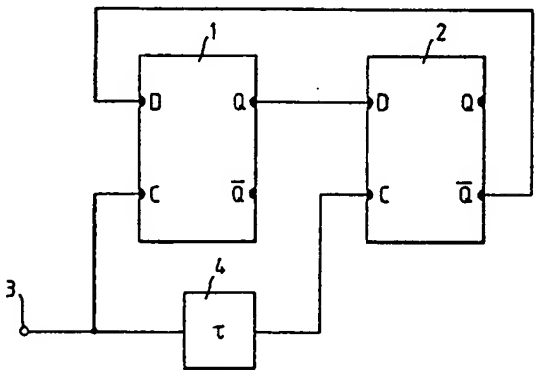
(72) Inventor: Murray, Bruce c/o Mullard Mitcham
2 New Road
Mitcham, Surrey CR4 4XY(GB)

(74) Representative: Cole, Bernard Victor et al
PHILIPS ELECTRONICS Patents and Trade Marks Department Centre Point New Oxford Street
London WC1A 1QJ(GB)

(54) Divider circuit.

(57) A pulse train divider circuit comprises a first flip-flop (1) whose Q output is connected to the D input of a second flip-flop (2) whose $\overline{Q}$ output is connected to the D input of the first flip-flop (1). A pulse train to be divided is applied via an input (3) directly to the clock input C of the first flip-flop (1) and via a circuit (4) which delays the pulse train applied to the clock input C of the flip-flop (2) to provide a given phase relationship between the pulse trains at the two clock inputs. The circuit divides-by-two and the resulting divided pulse trains available at the various outputs have phase relationships depending on the phase relationship of the applied pulse trains at the clock inputs.

Fig. 1.



EP 0 270 191 A2

"DIVIDER CIRCUIT"

The present invention relates to a pulse train divider circuit comprising first and second D-type flip-flops having the Q output of the first flip-flop connected to the D input of the second flip-flop whose $\overline{Q}$ output is connected to the D input of the first flip-flop, the pulse train to be divided being applied to the clock inputs of each of said flip-flops.

A divider circuit of the above type is disclosed in Electronic Letters, volume 18, number 13, dated 24th June, 1982, at page 581. This reference shows two D-type flip-flops connected and driven to produce divide-by-four outputs of fixed phase relationship.

It is an object of the invention to provide a divider circuit of the type described in the opening paragraph having a different divisor.

The invention provides a pulse train divider circuit comprising first and second D-type flip-flops having the Q output of the first flip-flop connected to the D input of the second flip-flop whose $\overline{Q}$ output is connected to the D input of the first flip-flop, the pulse train to be divided being applied to the clock inputs of each of said flip-flops, characterised in that said divider circuit additionally comprises means for causing the pulse train applied to one of said flip-flops to be out of phase with the pulse train as applied to the other of said flip-flops, the circuit being capable of providing a divided pulse train at each output of each flip-flop at half the frequency of the applied pulse train, the divided pulse train present at an output of the first flip-flop having a specific phase relationship with the divided pulse train at an output of the second flip-flop which relationship depends on the phase relationship between the pulse trains as applied to the clock inputs of the first and second flip-flops.

Such a divider circuit has the advantage that it can divide by two and in addition the phase relationship between two outputs can be selected, within limits, by controlling the phase relationship of the pulse train as applied to the clock inputs of the respective flip-flops.

When the means causes the pulse train applied to the clock input of the first flip-flop to lead the pulse train applied to the corresponding input of the second flip-flop by N degrees the divided pulse train at an output of the said first flip-flop leads the divided pulse train at the corresponding output of the second flip-flop by 1/2N degrees. In such a case the means can take the form of a delay circuit which can either by fixed or variable.

As an alternative, the means may comprise an inverter circuit provided in the connection of the pulse train to the clock input of one of the flip-flops, the divided pulse train at the output of said first flip-flop leading the divided pulse train at the corresponding output of the second flip-flop by 90 degrees. In such a case there is a 180 degrees phase difference between the pulse trains at the clock inputs of the respective flip-flops and it does not matter to which of these inputs the inverter is connected.

The above and other features of the invention will now be described, by way of example, with reference to the accompanying drawings in which:-

Figure 1 is a block diagram of a pulse train divider circuit according to the invention,

Figure 2 shows pulse diagrams for explaining the operation of Figure 1,

Figure 3 is a block diagram of a modification of the divider circuit shown in Figure 1,

Figure 4 shows pulse diagrams for explaining the operation of Figure 3,

Figure 5 is a block diagram of a further modification of the divider circuit shown in Figure 1, and

Figure 6 shows pulse diagrams for explaining the operation of Figure 5.

Figure 1 shows a first D-type flip-flop 1 connected to a second D-type flip-flop 2 such that the Q output of flip-flop 1 is connected to the D input of flip-flop 2 whose $\overline{Q}$ output is connected to the D input of flip-flop 1. The pulse train to be divided is applied by way of an input 3 directly to the clock input C of flip-flop 1 and via a circuit 4 to the clock input C of flip-flop 2. The circuit 4 changes the phase relationship, within limits, of the pulse train applied to the second flip-flop 2 with respect to that applied to the first flip-flop 1 and may take the form of a delay circuit.

The operation of the divider circuit of Figure 1 will be described with reference to the pulse diagrams of Figure 2 in which the two binary conditions, "1" and "0" respectively indicate the high and low conditions. In Figure 2 the inputs and outputs of the flip-flops are indicated in the normal way, the suffix "1" or "2" indicating that they relate respectively to the first or second flip-flop. Figure 2a shows the pulse train applied via input 3 directly to the clock input (C1) of flip-flop 1, the pulse train having a 1:1 mark:space ratio. Initially it is assumed in Figure 2b that the D input (D1) of flip-flop 1, and hence the $\overline{Q}$ output ($\overline{Q}$ 2) of flip-flop 2, is high with C1 low. When C1 next goes high flip-flop 1 changes state such that its Q output (Q1), which was previously low, goes high as shown in Figure 2c, there being a short delay in the flip-flop changing its state, with the result that the D input (D2) of flip-flop 2 becomes high. It is assumed that the circuit 4 delays the pulse train applied to terminal 3

such that there is a 90 degrees lag in the pulse train applied to the clock input (C2) of flip-flop 2, the pulse train at C2 being shown in Figure 2e. When C2 next goes high flip-flop 2 changes its state such that output $\overline{Q}$ 2 goes low with the result that input D1 goes low, there again being a short delay in the flip-flop changing state. Flip-flop 1 changes back to its other state on the next occasion that the pulse train at input C1 goes high to drive output Q1, and hence input D2, low. Flip-flop 2 then changes back to its other state when next the pulse train at input C2 goes high to drive output $\overline{Q}$ 2,and hence input D1, low. The cycle is then repeated. A change of state of each flip-flop occurs each time its clock input goes high with the result that the applied pulse train is divided-by-two. The outputs at the $\overline{Q}$ output ($\overline{Q}$ 1) for flip-flop 1 and the Q output (Q2) for flip-flop are additionally shown in Figures 2d and 2f respectively.

From the various output pulse trains shown in Figure 2 it will be seen that the outputs of flip-flop 1 have specific phase relationships with the outputs of flip-flop 2 and the divider circuit may be employed to provide two pulse trains with a specific phase relationship. Thus from Figure 2 it will be seen that when C1 leads C2 by 90 degrees:-

Q1 leads Q2 by 45 degrees
$\overline{Q}$ 1 leads $\overline{Q}$ 2 by 45 degrees
Q1 lags $\overline{Q}$ 2 by 135 degrees
$\overline{Q}$ 1 lags Q2 by 135 degrees.

Figure 3 shows a modification of the pulse train divider circuit shown in Figure 1 where corresponding references indicate corresponding components. In Figure 3 the circuit 4 is placed in the connection between terminal 3 and the clock input C of flip-flop 1 such that the applied pulse train at this clock input lags the corresponding input in flip-flop 2 by 90 degrees. Figure 4 shows the pulse diagrams for the operation of Figure 3 which use the same references as in Figure 2. This operation will not be described as it will be self-evident following on from the description surrounding Figure 1 and 2. From Figure 4 it will be seen that when C1 lags C2 by 90 degrees the following phase relationships exist at the flip-flop outputs:-

Q1 leads Q2 by 135 degrees
$\overline{Q}$ 1 leads $\overline{Q}$ 2 by 135 degrees
Q1 lags $\overline{Q}$ 2 by 45 degrees
$\overline{Q}$ 1 lags Q2 by 45 degrees.

A further modification of the pulse train divider circuit of Figure 1 is shown in Figure 5 where corresponding references again indicate like components. In Figure 5 the circuit 4 of Figure 1 has been replaced by an inverter 5 such that the pulse train applied to the clock input of flip-flop 1 leads the pulse train applied to the corresponding input of flip-flop 2 by 180 degrees. Figure 6 shows the pulse diagrams for the operation of Figure 5 which again uses the same references as in Figure 2. Again the operation will not be described as it will be self-evident. From Figure 6 it will be seen that when C1 leads C2 by 180 degrees the flip-flop outputs have the following phase relationships:-

Q1 leads Q2 by 90 degrees
$\overline{Q}$ 1 leads $\overline{Q}$ 2 by 90 degrees
Q1 lags $\overline{Q}$ 2 by 90 degrees
$\overline{Q}$ 1 lags Q2 by 90 degrees.

The same relationships are also obtained if the inverter 5 is provided in the connection to the clock input C of flip-flop 2 rather than flip-flop 1.

Claims

1. A pulse train divider circuit comprising first and second D-type flip-flops having the Q output of the first flip-flop connected to the D input of the second flip-flop whose $\overline{Q}$ output is connected to the D input of the first flip-flop, the pulse train to be divided being applied to the clock inputs of each of said flip-flops, characterised in that said divider circuit additionally comprises means for causing the pulse train applied to one of said flip-flops to be out of phase with the pulse train as applied to the other of said flip-flops, the circuit being capable of providing a divided pulse train at each output of each flip-flop at half the frequency of the applied pulse train, the divided pulse train present at an output of the first flip-flop having a specific phase reltationship with the divided pulse train at an output of the second flip-flop which relationship depends on the phase relationship between the pulse trains as applied to the clock inputs of the first and second flip-flops.

2. A divider circuit as claimed in Claim 1, characterised in that when said means causes the pulse train applied to the clock input of the first flip-flop to lead the pulse train applied to the corresponding input of the second flip-flop by N degrees the divided pulse train at an output of the said first flip-flop leads the divided pulse train at the corresponding output of the second flip-flop by 1/2N degrees.

3. A divider circuit as claimed in Claim 1, characterised in that said means comprises an inverter circuit provided in the connection of the pulse train to the clock input of one of the flip-flops, the divided pulse train at the output of said first flip-flop leading the divided pulse train at the corresponding output of the second flip-flop by 90 degrees.

Fig.1.

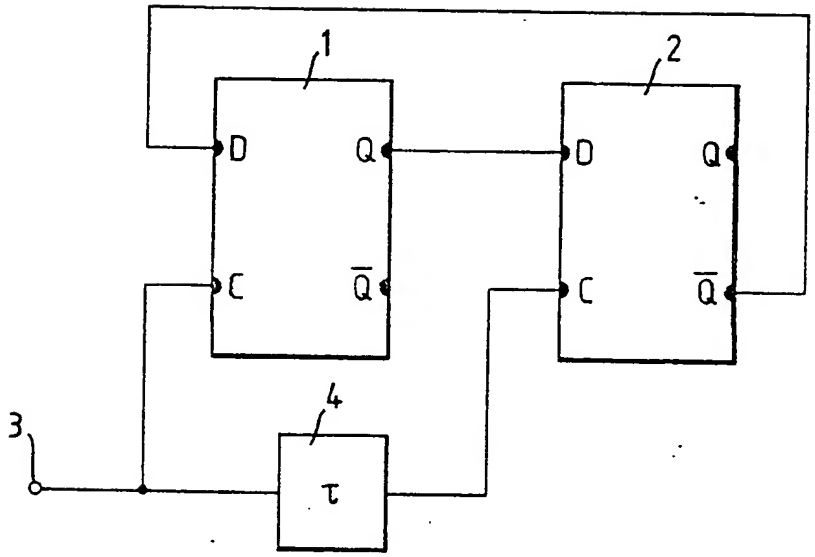

1
2
D
Q
C
$\overline{Q}$
D
Q
C
$\overline{Q}$
3
4
τ

Fig.2.

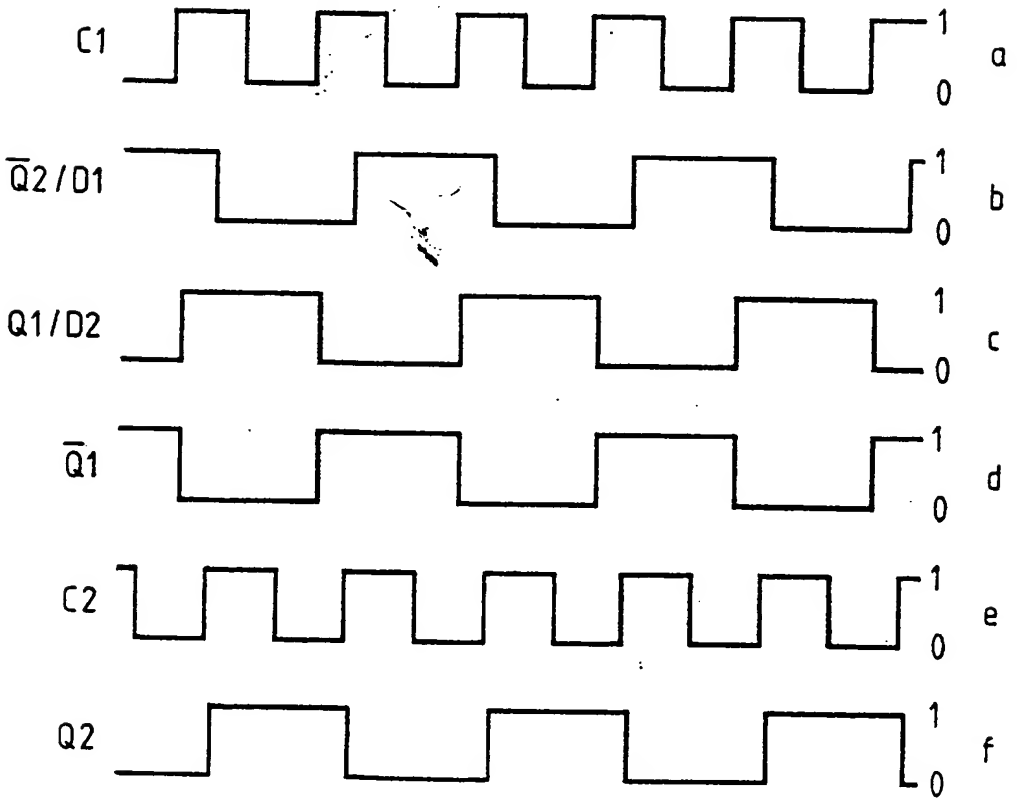

C1
1
0
a
$\overline{Q}$2/D1
1
0
b
Q1/D2
1
0
c
$\overline{Q}$1
1
0
d
C2
1
0
e
Q2
1
0
f

Fig.3.

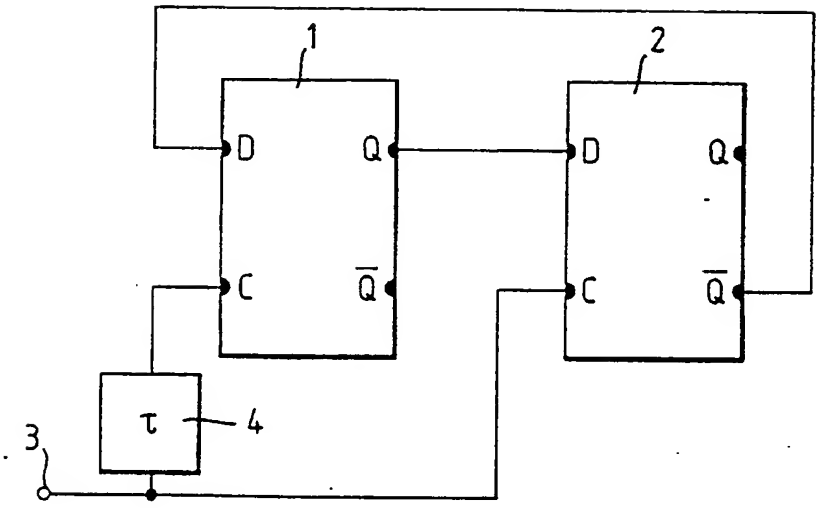

1
2
D
Q
D
Q
C
$\overline{Q}$
C
$\overline{Q}$
τ
4
3

Fig.4.

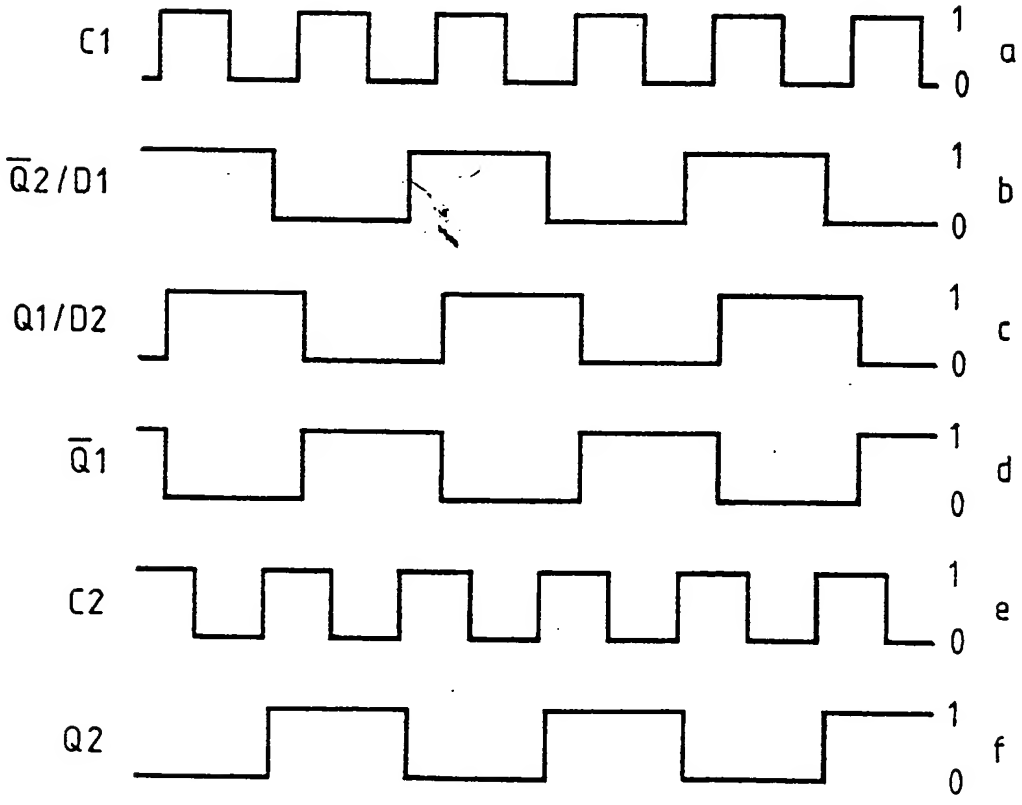

C1
1
0
a
$\overline{Q}$2/D1
1
0
b
Q1/D2
1
0
c
$\overline{Q}$1
1
0
d
C2
1
0
e
Q2
1
0
f

Fig.5.

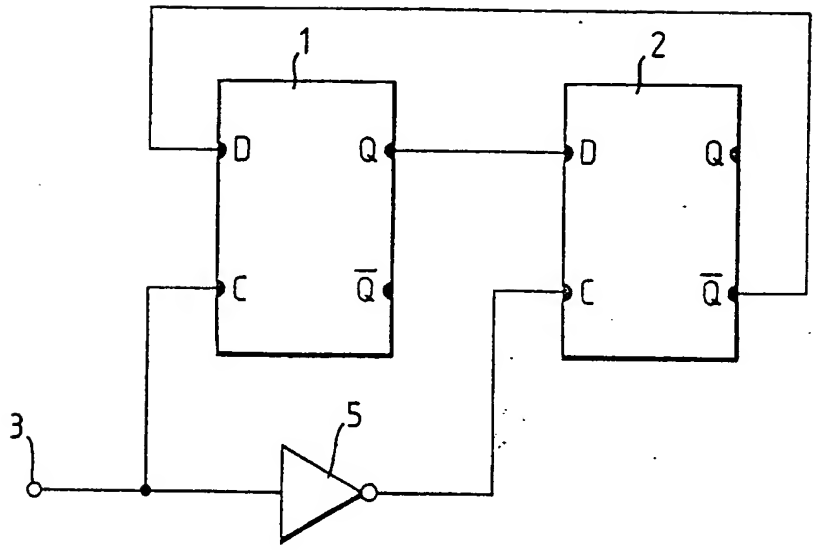
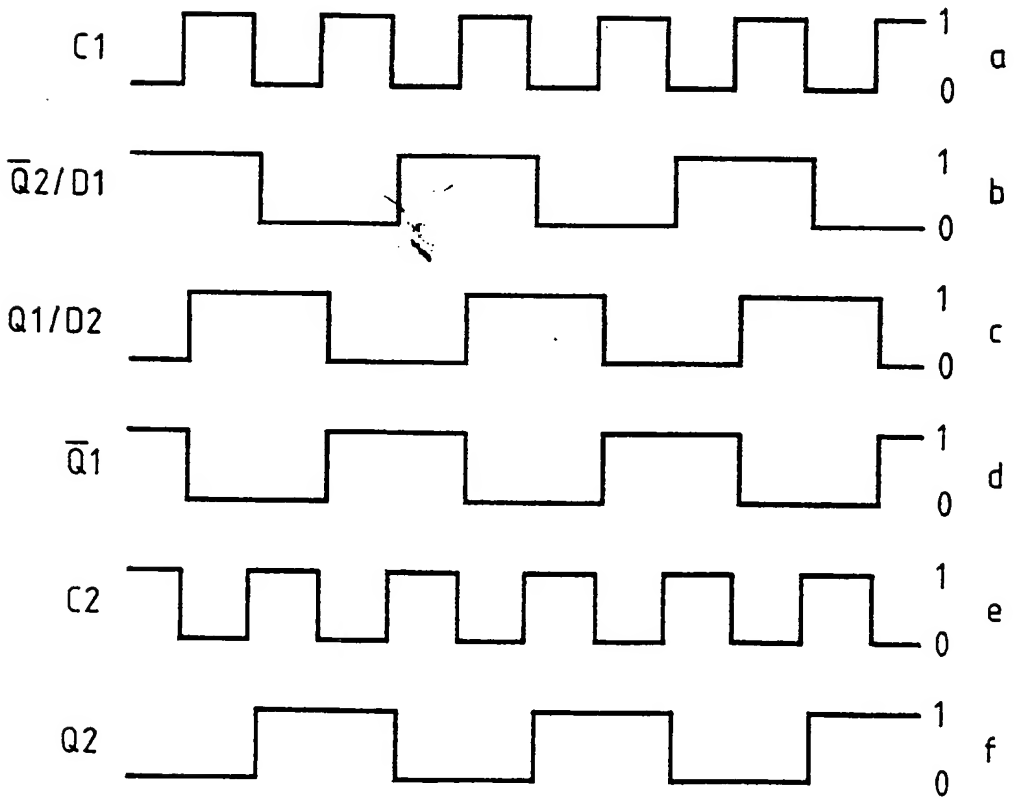

1
2
D
Q
D
Q
C
$\overline{Q}$
C
$\overline{Q}$
3
5

Fig.6.


C1
1
0
a
$\overline{Q}$2/D1
1
0
b
Q1/D2
1
0
c
$\overline{Q}$1
1
0
d
C2
1
0
e
Q2
1
0
f

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 270 191**
A3

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: 87202388.2

(51) Int. Cl.4: H03K 23/00 , H03K 5/15

(22) Date of filing: 02.12.87

(30) Priority: 05.12.86 GB 8629108

(43) Date of publication of application:
08.06.88 Bulletin 88/23

(84) Designated Contracting States:
DE FR GB IT NL

(88) Date of deferred publication of the search report:
14.06.89 Bulletin 89/24

(71) Applicant: PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED
Philips House 188 Tottenham Court Road
London W1P 9LE(GB)

(84) GB

Applicant: N.V. Philips' Gloeilampenfabrieken
Groenewoudseweg 1
NL-5621 BA Eindhoven(NL)

(84) DE FR IT NL

(72) Inventor: Murray, Bruce c/o Mullard Mitcham
2 New Road
Mitcham, Surrey CR4 4XY(GB)

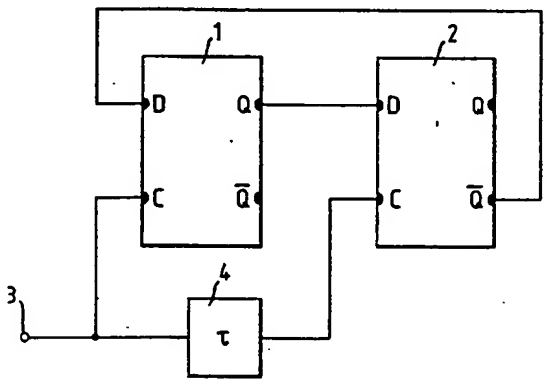
(74) Representative: Cole, Bernard Victor et al
PHILIPS ELECTRONICS Patents and Trade Marks Department Centre Point New Oxford Street
London WC1A 1QJ(GB)

(54) **Divider circuit.**

(57) A pulse train divider circuit comprises a first flip-flop (1) whose Q output is connected to the D input of a second flip-flop (2) whose $\overline{Q}$ output is connected to the D input of the first flip-flop (1). A pulse train to be divided is applied via an input (3) directly to the clock input C of the first flip-flop (1) and via a circuit (4) which delays the pulse train applied to the clock input C of the second flip-flop (2) to provide a given phase relationship between the pulse trains at the two clock inputs. The circuit divides-by-two and the resulting divided pulse trains available at the various outputs have phase relationships depending on the phase relationship of the applied pulse trains at the clock inputs.

The delay circuit (4) may be an inverter giving 180° phase delay.

Fig.1.



EP 0 270 191 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 87 20 2388

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	US-A-4 420 696 (K. GEMMA et al.) * figure 9, elements 42,43,41 (invertermeans); column 6, lines 7-27; figure 10, waveforms CL1,CL2, CL3,CL8 (not shown); figure 9, elements 44,45; column 6, lines 27-40; figure 10, waveforms CL4, CL3,CL5,CL6 *	1-3	H 03 K 23/00 H 03 K 5/15
X	PHILIPS TECHNISCHE RUNDSCHAU vol. 38, no. 2, 1979, pages 47-62, Eindhoven,D; W.D. KASPERKOVITZ:"Frequenzteiler für ultrahohe Frequenzen." * figure 1 *	1-3	
P,X	DE-A-3 546 132 (ANT NACHRICHTENTECHNIK GMBH) * figure 3; figures 4 A - 4 C; abstract; claims 1,2; column 2, lines 41-54 *	1-3	
A	ELECTRONIC ENGINEERING vol. 48, no. 584, October 1976, pages 29,30; P. MISRA et al.:"Control clocks for a four phase stepper motor." * figures 1,2 *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 03 K 5/15 H 03 K 23/00 H 03 K 23/54
A	EP-A-0 189 744 (LIGNES TELEGRAPHIQUES ET TELEPHONIQUES L.T.T.) * figures 7,8; page 5, lines 14-34 *	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	13-03-1989	ARENDT M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)